# Tutorial 4: WRES1201 Computer System Architecture

1. What is the general relationship among access time, memory cost and capacity?
2. What are the differences among *direct mapping*, *associative mapping* and *set associative mapping*?
3. Consider a machine with a byte addressable main memory of 216 bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.
   1. How is a 16-bit memory address divided into tag, line number, and byte number?
   2. Into what line would bytes with each of the following addresses be stored?
      1. 0001 0001 0001 1011
      2. 1100 0011 0011 0100
      3. 1101 0000 0001 1101
      4. 1010 1010 1010 1010
   3. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the bytes stored along with it?
   4. How many total bytes of memory can be stored in the cache?
   5. Why is the tag also stored in the cache?
4. A cache has 64KB capacity, 128byte per lines and is 4-way set-associative. The system containing the cache uses 32-bit addresses. How many lines and sets does the cache have?
5. Describes three method used by cache memory to do replacement policy?
6. What are the differences between write-through and write-back?
7. Consider a direct mapping single-level cache with an access time of 2.5ns, a line size of 64 bytes, and a hit ration of H= 0.95. Main memory uses a block transfer capability that has first-word (4 bytes) access time of 50ns and an access time of 5 ns for each word thereafter.
   1. What is the access time when there is a cache miss? Assume that the cache waits until the line has been fetched from main memory and then re-executes for a hit.
   2. Suppose that increasing the line size to 128 bytes increases the H to 0.97. Does this reduce the average memory access time?

1. For a system with two levels of cache, define Tc1 = first level cache access time; Tc2 = second level cache access time; Tm = main memory access time; H1 = first level hit ratio; H2 = combined first/second level hit ratio. Provide an equation for Ta for a read operation.